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09/511,986	02/24/2000	Vernon M. Williams	4208US (99-0316)	6129

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EXAMINER	
NADAV, ORI	

ART UNIT	PAPER NUMBER
2811	

DATE MAILED: 11/03/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 09/511,986	Applicant(s) WILLIAMS, VERNON M.
	Examiner ori nadav	Art Unit 2811

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *25 August 2003* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *47,48,50-56,58-68,75-90 and 110-124* is/are pending in the application.

4a) Of the above claim(s) *80 and 86-90* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *47,48,50-56,58-68,75-79,81-85 and 110-124* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) *31,32* .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Information Disclosure Statement

1. The Information Disclosure Statement filed on 5/08/2003 has been considered.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

The changes made to 35 U.S.C. 102(e) by the American Inventors Protection Act of 1999 (AIPA) and the Intellectual Property and High Technology Technical Amendments Act of 2002 do not apply when the reference is a U.S. patent resulting directly or indirectly from an international application filed before November 29, 2000. Therefore, the prior art date of the reference is determined under 35 U.S.C. 102(e) prior to the amendment by the AIPA (pre-AIPA 35 U.S.C. 102(e)).

2. Claims 64-66, 68, 75, 77-79 and 81-83 are rejected under 35 U.S.C. 102(e) as being anticipated by Matsuki et al. (5,969,424).

Regarding claim 64, Matsuki et al. teach in figure 2 and related text (column 6, line 51 to column 7, line 37) a semiconductor device assembly, comprising: a carrier 11, 12 (column 7, lines 28-30) including contacts and carrying circuitry in communication with the contacts; and at least one semiconductor die 1, 2 adjacent the carrier, the semiconductor die including bond pads 4 (see plurality of bond pads in figure 1); arid conductive elements 7 (see plurality of conductive elements 7 in figure 1) extending between and contacting contacts 11 (column 7, line 30) of the carrier and corresponding bond pads 4 to electrically connect circuitry of the at least one semiconductor die with the circuitry of the carrier, each of the conductive elements 7 including a plurality of superimposed, contiguous, mutually adhered layers 13, 15, each of the layers comprising copper, a conductive material (column 8, lines 31-34).

Although Matsuki et al. do not all electronic circuit element 2 a semiconductor die, electronic circuit element 2 is a semiconductor device, thus rendering it a semiconductor chip.

Note that conductive elements 7 electrically connect contacts 11 of the carrier to corresponding bond pads 4, because during bonding contacts 11 are connected to bumps 10 (column 9, lines 11-15).

Regarding claim 75, Matsuki et al. teach in figure 2 substantially the entire claimed structure, as applied to claim 64 above, wherein the part of layer 11 contacting bump 10 during bonding is the at least one contact pad 11, and thus

the at least one conductive element is in contact with both first and second contact pads.

Regarding claim 65, although Matsuki et al. do not categorize film carrier as a carrier substrate, a film carrier is synonymous to a carrier substrate.

Regarding claim 66, Matsuki et al. teach in figure 2 a carrier comprises leads 11 (column 7, line 30).

Regarding claims 68 and 77, Matsuki et al. teach in figure 2 conductive material comprises a metal (column 8, lines 58-61).

Regarding claims 78-79, Matsuki et al. teach in figure 2 at least one of the first and second semiconductor device components comprises a packaged semiconductor die 2.

Regarding claim 81, Matsuki et al. teach in figure 2 at least one of the first and second semiconductor device components comprises a carrier substrate 11, 12.

Regarding claim 82, Matsuki et al. teach in figure 2 a carrier substrate includes a support structure 12 and at least one conductive element 7 in communication with the at least one contact pad 11 thereof. Layer 12 is a support structure,

because during bonding contacts 11 are connected to bumps 10, and the substrate supports chip 2.

Regarding claim 83, Matsuki et al. teach in figure 2 at least one of the at least one conductive element 7 and the support structure 12 comprises a plurality of superimposed, contiguous, mutually adhered layers 13, 15, 16 of material.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 47-48, 50-56, 58-63, 67, 76 and 110-124 are rejected under 35 U.S.C. 103(a) as being unpatentable over Matsuki et al. in view of Lee et al. (4,954,873).

Regarding claims 47, 48, 52, 56, 67, 76, 110, 111, 114, 115 and 118, Matsuki et al. teach in figures 1 and 2 and related text substantially the entire claimed structure, as applied to claims 64 and 75 above, except a conductive trace (synonymous to the a "conductive material") comprises a polymer of a thermoplastic conductive elastomer.

Lee et al. teach in figure 5 and related text a conductive trace/material 22 comprises a polymer of a thermoplastic conductive elastomer (column 6, line 7).

It would have been obvious to a person of ordinary skill in the art at the time the invention was made to use a conductive trace comprises a polymer of a thermoplastic conductive elastomer, as taught by Lee et al., in Matsuki et al.'s device in order to reduce the complexity of the bonding process since the elastomer conforms more closely to the contours of the device surface, and in order to improve the device reaction to thermally induced stress and strain pressures. The combination is motivated by the teachings of Lee et al. who point out the advantages of using a conductive trace comprises a polymer of a thermoplastic conductive elastomer (column 2, line 53 to column 3, line 5) and who further point out that polymers of a thermoplastic conductive elastomer are particularly suitable for interfacing between electronic devices having arrays of electrical contact pads (abstract).

Regarding the claimed limitations of at least a portion of the conductive trace being configured to extend and conduct electrical signals along a plane which is parallel to a plane in which the at least one semiconductor device component is located, Matsuki et al. teach in figure 2 a conductive trace being configured to extend and conduct electrical signals along two planes which are perpendicular to one another. Therefore, although Lee et al. teach a thermoplastic conductive elastomer conduct electrical signals perpendicular to the plane of the semiconductor device, when combining Lee et al. with Matsuki et al., at least one of the two planes of the conductive trace will conduct electrical signals along a plane which is parallel to a plane in which the at least one semiconductor device component is located,

Regarding claims 50, 51, 53, 112 and 113 Matsuki et al. teach in figure 2 a conductive trace of claim 47, configured to be carried by a single semiconductor device component 1, 2 and configured to at least partially electrically connect two semiconductor device components 1, 2 and 11, 12, and substantially entirely carried by the semiconductor device component 1, 2, respectively.

Regarding claims 54, 59, 116 and 120, Matsuki et al. teach in figure 2 a semiconductor device component 11, 12 comprises a layer of a carrier substrate.

Regarding claims 55 and 117, Matsuki et al. teach in figure 2 a semiconductor device component comprises a dielectric layer 5 disposed on an active surface of a semiconductor die.

Regarding claims 58 and 119, Matsuki et al. teach in figure 2 at least one conductive trace 7 communicates with a contact 4 of the semiconductor device component.

Regarding claims 60, 61, 121 and 122, Matsuki et al. teach in figure 2 semiconductor device components 1, 2 comprise a semiconductor die and a packaged semiconductor device.

Regarding claims 62, 63, 123 and 124, Matsuki et al. teach in figure 2 semiconductor device component comprises leads 11 (column 7, line 29), wherein the at least one conductive element 7 contacts one of the leads.

Claims 75 and 84-85 are rejected under 35 U.S.C. 103(a) as being unpatentable over Congleton et al. (5,007,576) in view of Matsuki et al.
Regarding claims 75 and 84-85, Congleton et al. teach in figure 1e and related text a semiconductor device assembly comprising a first semiconductor device component 10 including at least one contact pad 10a (see figure 1c); a second semiconductor device component 30 including at least one contact pad 30a; and at least one conductive element 16 (see figure 1c) connecting the at least one contact pad of the first semiconductor device component to the at least one contact pad of the second semiconductor device component, wherein at least one conductive element 16 is located on a surface of each of the first 10 and second 30 semiconductor device components, and wherein the at least one conductive element 16 extends across a peripheral edge of at least one of the first and second semiconductor device components (column 4, lines 5-9 and column 5, lines 7-27).
Congleton et al. do not teach at least one conductive element comprising a plurality of superimposed, contiguous, mutually adhered layers comprising conductive material.
Matsuki et al. teach in figure 2 and related text at least one conductive element 7 comprising a plurality of superimposed, contiguous, mutually adhered layers 13,

15, each of the layers comprising copper, a conductive material (column 8, lines 31-34).

It would have been obvious to a person of ordinary skill in the art at the time the invention was made to use at least one conductive element comprising a plurality of superimposed, contiguous, mutually adhered layers comprising conductive material, as taught by Matsuki et al., in Congleton et al.'s device in order to improve the adhesion between the conductive element and the surfaces there under, while providing good conductor conductivity. The combination is motivated by the teachings of Matsuki et al. who point out the advantages of using a conductive element comprising a plurality of superimposed, contiguous, mutually adhered layers comprising conductive material (column 7, line 65 to column 8, line 44).

Response to Arguments

4. Applicant argues that lead wires 7 of Matsuki et al. do not contact both contact pads 4 and 11.

Conductive elements 7 electrically connect contacts 11 of the carrier to corresponding bond pads 4, because during bonding contacts 11 are connected to bumps 10 (column 9, lines 11-15).

Applicant argues that the device of Matsuki et al. and Lee et al. do not include the claimed limitations of at least a portion of the conductive trace being

configured to extend and conduct electrical signals along a plane which is parallel to a plane in which the at least one semiconductor device component is located, because Lee et al. teach a thermoplastic conductive elastomer conduct electrical signals perpendicular to the plane of the semiconductor device.

Matsuki et al. teach in figure 2 a conductive trace being configured to extend and conduct electrical signals along two planes which are perpendicular to one another. Therefore, although Lee et al. teach a thermoplastic conductive elastomer conduct electrical signals perpendicular to the plane of the semiconductor device, when combining Lee et al. with Matsuki et al., at least one of the two planes of the conductive trace will conduct electrical signals along a plane which is parallel to a plane in which the at least one semiconductor device component is located,

Papers related to this application may be submitted to Technology center (TC) 2800 by facsimile transmission. Papers should be faxed to TC 2800 via the TC 2800 Fax center located in Crystal Plaza 4, room 4-C23. The faxing of such papers must conform with the notice published in the Official Gazette, 1096 OG 30 (November 15, 1989). The Group 2811 Fax Center number is (703) 308-7722 and 308-7724. The Group 2811 Fax Center is to be used only for papers r lated to Group 2811 applications.

Any inquiry concerning this communication or any earlier communication from the Examiner should be directed to *Examiner Nadav* whose telephone number is **(703) 308-8138**. The Examiner is in the Office generally between the hours of 7 AM to 4 PM (Eastern Standard Time) Monday through Friday.

Any inquiry of a general nature or relating to the status of this application should be directed to the **Technology Center Receptionists** whose telephone number is **308-0956**

O.N.
October 29, 2003

ORI NADAV
PATENT EXAMINER
TECHNOLOGY CENTER 2800